YAMAHA LSI

# YMF289B

## OPL3-L

### OPL3 Low Voltage version

## ■ OVERVIEW

YMF289B (OPL3-L) is a synthesizer chip developed specially for note PC, PCMCIA (type II) card. YMF289B is compatible with YMF262 which is de facto standard in sound card market. Special functions (power down mode, 3.3V power supply and etc.) are newly featured.

## ■ FEATURES

- Register-compatible with YMF262
  1. Sound generation modes
     - Two-operator mode
       Generates eighteen voices or fifteen voices plus five rhythm sounds simultaneously.
     - Four-operator mode
       Generates six voices in four-operator mode plus six voices in two-operator mode, or generates six voices in four-operator mode plus three voices in two-operator mode plus five rhythm sounds simultaneously.
  2. Eight selectable waveforms
  3. Stereo output
- Sampling frequency is 44.1kHz.
- All registers are readable.
- Supports low power consumption mode (power down mode).
- 5V or 3.3V power supply.
- DAC interface compatible with YAC516 and YAC513.
- 44-pin QFP (YMF289B-F) or 48-pin SQFP (YMF289B-S) package.

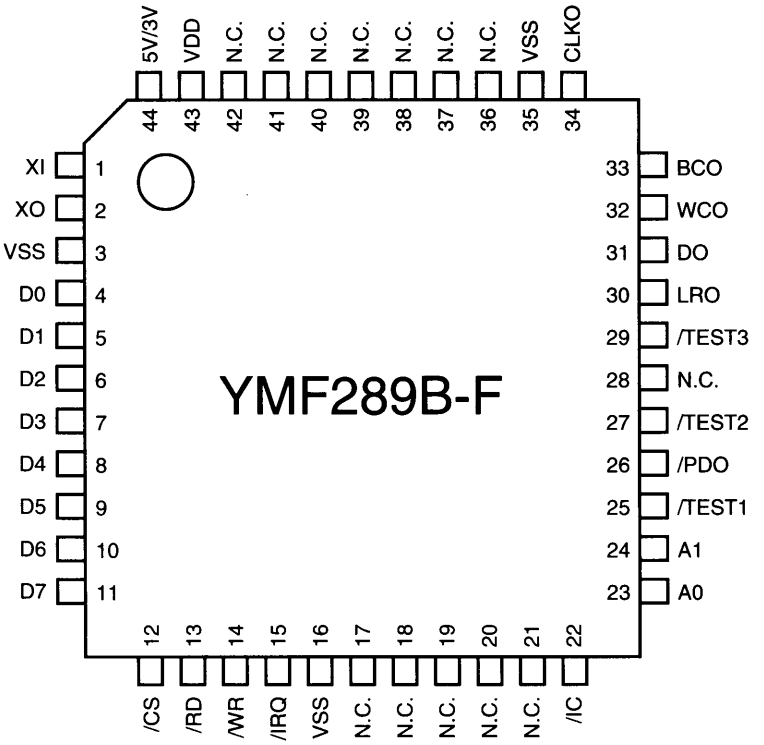
YAMAHA CORPORATION

| YMF289B CATALOG |
| --- |
| CATALOG No.: LSI-4MF289B2 |
| 1995. 3 |


找芯片 维库一下 www.dzsc.com

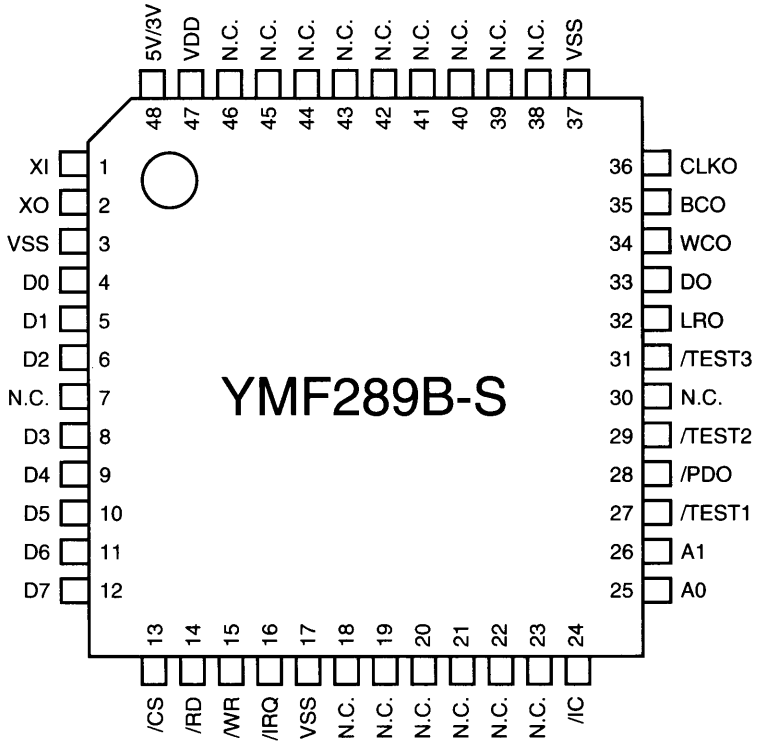
## ■ PIN OUT DIAGRAM

### • YMF289B-F




44 pin Top View

### • YMF289B-S




48 pin Top View

找芯片 维库一下 www.dzsc.com

## ■ PIN DESCRIPTION

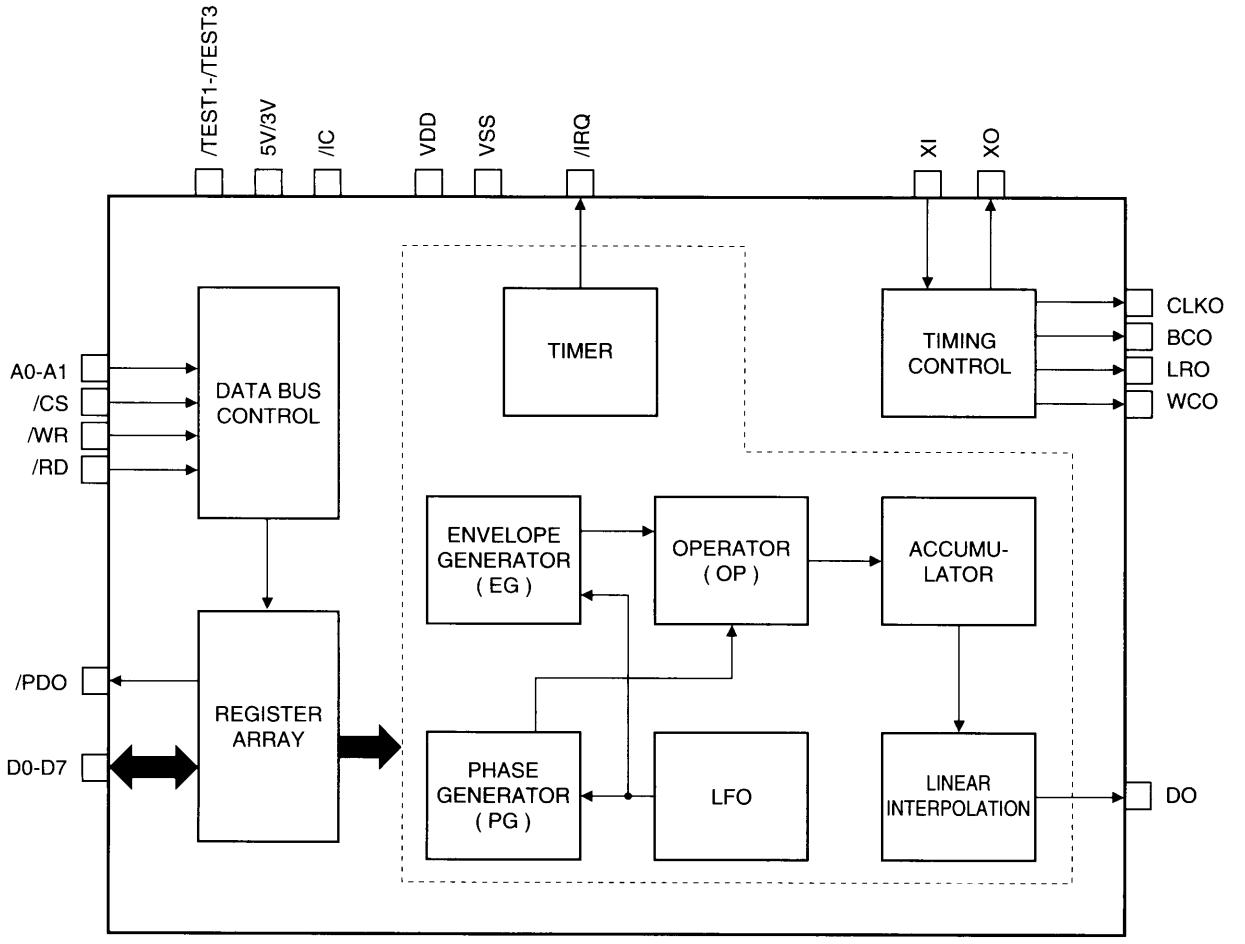
| No. | | I/O | Name | Function |
|---|---|---|---|---|
| 44QFP | 48SQFP | | | |
| 1 | 1 | I | XI | Crystal oscillator connection pin or master clock input (33.8688MHz) |
| 2 | 2 | O | XO | Crystal oscillator connection pin |
| 3 | 3 | - | VSS | Ground |
| 4 | 4 | I/O | D0 | CPU interface: data 0 |
| 5 | 5 | I/O | D1 | CPU interface: data 1 |
| 6 | 6 | I/O | D2 | CPU interface: data 2 |
| 7 | 8 | I/O | D3 | CPU interface: data 3 |
| 8 | 9 | I/O | D4 | CPU interface: data 4 |
| 9 | 10 | I/O | D5 | CPU interface: data 5 |
| 10 | 11 | I/O | D6 | CPU interface: data 6 |
| 11 | 12 | I/O | D7 | CPU interface: data 7 |
| 12 | 13 | I | /CS | CPU interface: chip select |
| 13 | 14 | I | /RD | CPU interface: read enable |
| 14 | 15 | I | /WR | CPU interface: write enable |
| 15 | 16 | OD | /IRQ | CPU interface: interrupt signal |
| 16 | 17 | - | VSS | Ground |
| 22 | 24 | I+ | /IC | Initial clear input |
| 23 | 25 | I | A0 | CPU interface: address 0 |
| 24 | 26 | I | A1 | CPU interface: address 1 |
| 25 | 27 | I+ | /TEST1 | LSI test pin (Normally NC) |
| 26 | 28 | O | /PDO | Power down mode output |
| 27 | 29 | I+ | /TEST2 | LSI test pin (Normally NC) |
| 29 | 31 | I+ | /TEST3 | LSI test pin (Normally NC) |
| 30 | 32 | O | LRO | DAC interface: L/R clock output |
| 31 | 33 | O | DO | DAC interface: voice data output |
| 32 | 34 | O | WCO | DAC interface: word clock output |
| 33 | 35 | O | BCO | DAC interface: bit clock output |
| 34 | 36 | O | CLKO | Clock output pin (16.9344MHz) |
| 35 | 37 | - | VSS | Ground |
| 43 | 47 | - | VDD | +5V (or +3.3V) power supply |
| 44 | 48 | I | 5V/3V | 5V, 3.3V operation select (H: 5V, L:3.3V) |

All pins other than the above are N.C. Normally do not connect them.

Note) I+: Input pin with pull up resistor
OD: Open drain output pin

维库一下 www.dzsc.com

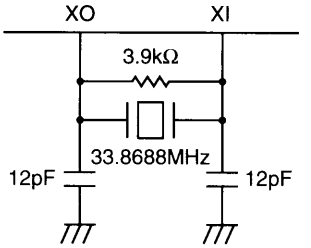
## ■ BLOCK DIAGRAM




## ■ FUNCTION OVERVIEW

### 1. Master clock

The YMF289B synthesized frequency and envelope rate depend on the clock supplied from the XI pin. The YMF289B has a built-in self-oscillation circuit. Therefore, connect a 33.8688MHz (third overtone oscillation) crystal oscillator to the XI and XO pins as shown below.






找芯片 维库一下 www.dzsc.com

## 2. CPU interface

The FM performance, sound generation, and other functions of the YMF289B are controlled by writing data to the data registers described in "3. Register map". Data is written to and read from the registers over the data bus (D0 to D7). The data bus is controlled by address signals A0 and A1 and control signals /CS, /WR, and /RD. These signals set the data bus mode as shown below.

| /CS | /RD | /WR | A1 | A0 | Mode |
|---|---|---|---|---|---|
| H | X | X | X | X | Interactive mode |
| L | L | H | L | L | Status read mode |
| L | H | L | L/H | L | Address write mode |
| L | H | L | X | H | Data write mode |
| L | L | H | X | H | Data read mode |

X: Don't care

### 2-1 Inactive Mode

When /CS is 'H', data bus (D0-D7) becomes high-impedance.

### 2-2 Status Read Mode

The Status Register can be read from D0-D7 in this mode.

### 2-3 Address Write Mode

In this mode data presented at D0-D7 will be latched as the register to be accessed. The A1 signal determines which register array is accessed: when A1 is 'L', register array 0 is selected: when A1 is 'H', register array 1 is selected.

*<Caution>*

*Do not attempt to use the latched address until 56 (master clock) cycles have elapsed.*

### 2-4 Data Write Mode

Data written to D0-D7 will go to the previously specified register. Successive writes to the same register can be made without refreshing the address.

*<Caution>*

*Do not attempt to change the latched address or write new data until 56 (master clock) cycles have elapsed.*

### 2-5 Data Read Mode

The previously specified register can be read from D0-D7 in this mode.

维库一下 www.dzsc.com

## 3. Register map

The YMF289B registers are made up of data registers, which control the LSI itself, and status registers, which show the status of the LSI.
Most of the data registers are compatible with the YMF262(OPL3). The YMF289B can read all the registers, even those not supported by the YMF262. However, the registers cannot be read in the power down mode. Initialization (/IC="L") clears all the registers.

### 3-1 Data registers

| ADDRESS | REGISTER ARRAY 0 (A1='L') | | | | | | | | REGISTER ARRAY 1 (A1='H') | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (HEX) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 00H~01H | LSI TEST | | | | | | | | LSI TEST | | | | | | | |
| 02H | TIMER 1 | | | | | | | | | | | | | | | |
| 03H | TIMER 2 | | | | | | | | | | | | | | | |
| 04H | RST | MT1 | MT2 | | | | ST2 | ST1 | | | CONNECTION SEL | | | | | |
| 05H | | | | | | | | | | | | | | NEW3 | ★ | NEW |
| 08H | | NTS | | | | | | | | | | | | CLR | PD1 | PD0 |
| 20H~35H | AM | VIB | EGT | KSR | MULT | | | | AM | VIB | EGT | KSR | MULT | | | |
| | | | | | 3 | 2 | 1 | 0 | | | | | 3 | 2 | 1 | 0 |
| 40H~55H | KSL | | TL | | | | | | KSL | | TL | | | | | |
| | 1 | 0 | 5 | 4 | 3 | 2 | 1 | 0 | 1 | 0 | 5 | 4 | 3 | 2 | 1 | 0 |
| 60H~75H | AR | | | | DR | | | | AR | | | | DR | | | |
| | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| 80H~95H | SL | | | | RR | | | | SL | | | | RR | | | |
| | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 | 3 | 2 | 1 | 0 |
| A0H~A8H | F-NUMBER (L) | | | | | | | | F-NUMBER (L) | | | | | | | |
| | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 |
| B0H~B8H | | | KON | BLOCK | | | F-NUM (H) | | | | KON | BLOCK | | | F-NUM (H) | |
| | | | | B2 | B1 | B0 | F9 | F8 | | | | B2 | B1 | B0 | F9 | F8 |
| BDH | DAM | DVB | RHY | BD | SD | TOM | TC | HH | | | | | | | | |
| C0H~C8H | ★ | ★ | CHR | CHL | FB | | | CNT | ★ | ★ | CHR | CHL | FB | | | CNT |
| | | | | | FB2 | FB1 | FB0 | | | | | | FB2 | FB1 | FB0 | |
| E0H~F5H | | | | | | WS | | | | | | | | WS | | |
| | | | | | | W2 | W1 | W0 | | | | | | W2 | W1 | W0 |

Notes)

1. The register map is basically the same as that of the YMF262 except for the following:
   a) The NEW3, PD0, PD1, and CLR bits of registers 05H and 08H of REGISTER ARRAY 1 are newly defined.
   b) Bits D6 and D7 of registers C0 to C8H of register arrays 0 and 1 are not supported .
2. The LSI TEST registers are used for factory testing. Always set them to "0" during normal operation.
3. ☐ not used by the YMF289B may be used to expand the functions. Always set them to "0".
4. Bits indicated by ★ can be read, but are not supported functionally.



找芯片 维库一下 www.dzsc.com

### 3.2 Status register

| ADDRESS (HEX) | STATUS REGISTER | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| xx | IRQ | FT1 | FT2 | | | BUSY | | BUSY |

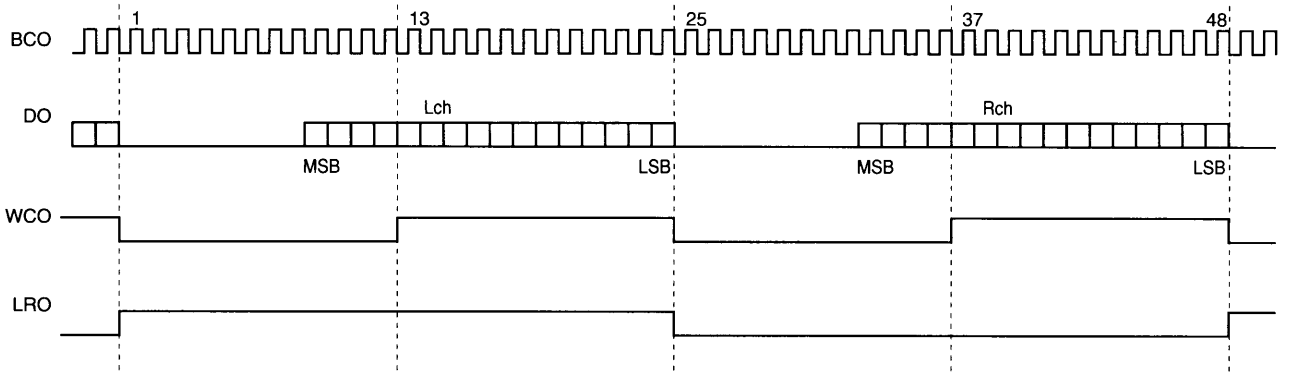
**YMF289B identification**

When the status is read after initialization, the YM3812(OPL2) outputs 06H and the YMF262 outputs 00H.

The YMF289B outputs the same value as the YMF262, but since it can read all the data registers, it can be discriminated from the YMF262 by whether or not all the data registers can be read.

## 4. DAC interface

The YMF289B outputs the voice data as digital data. Therefore, an external D/A converter is necessary. The digital data is output MSB-first from the DO pin as 2's complement data. The sampling frequency is 44.1kHz. The relationship between the DO pin digital data and the control signals (BCO, WCO, LRO) is shown below.




BCO: 48fs duty 50%
WCO: 2fs duty 50%
LRO: fs duty 50%

## 5. Additional functions

The YMF289B has the following additional functions, as compared to the YMF262.

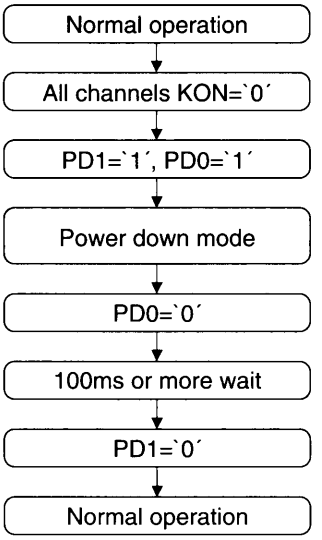
### 5-1 NEW3 bit

This bit enables the newly defined bits (PD0 bit, PD1 bit, CLR bit, BUSY flag). When this bit is "1", the bits above are enabled.

维库一下 www.dzsc.com

### 5-2 PD0, PD1 bits

These bits set the power down mode. Always set and reset the power down mode in the following order:




**Power down mode**

In the power down mode, clock oscillation is completely stopped and there is much lower power consumption than during normal operation. At this time, synthesizing stops, but the registers retain their contents before the YMF289B enters the power down mode.

In the power down mode, all the DAC interface pins (CLKO, LRO, WCO, BCO, DO) are fixed at the "L" level and the /IRQ pin retains its state before the YMF289B enters the power down mode. Be sure to fix the input pins (including D0 to D7) at the "H" or "L" level.

*<Caution>*

*If KON="1" when the machine returns from the power down mode, unexpected sound may be generated. Therefore, before switching to the power down mode, set all channels to KON="0". As for the timer, when the machine returns from the power down mode, RST becomes "1" and the counter is reset.*

### 5-3 CLR bit

This bit clears all the data register bits except NEW and NEW3. CLR="1" clears the data registers and CLR="0" resets the data registers. The time required to clear the data registers is 90µs (3000 cycles @ 33.8688NHz).

### 5-4 BUSY flag

This flag inhibits register access. It remains "1" until the data bus data is latched as an address, or is verified as register data.

### 5-5 /PDO pin

This bit becomes "L" when the YMF289B shifted to the power down mode. When the YMF289B returns to normal operation, this bit becomes "H". Use this bit to control a YAC516 or other YMF289B peripheral LSI.

找芯片 维库一下 www.dzsc.com

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute maximum ratings

| Item | Symbol | Rated value | Unit |
|---|---|---|---|
| Power supply voltage | $V_{DD}$ | –0.3~7.0 | V |
| Input voltage | $V_{IN}$ | –0.3~$V_{DD}$+0.5 | V |
| Operation temperature | $T_{OP}$ | 0~70 | °C |
| Storage temperature | $T_{STG}$ | –50~125 | °C |

### 2. Recommended operating conditions

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{DD}$ | 5V/3V="H" | 4.75 | 5.00 | 5.25 | V |
| | $V_{DD}$ | 5V/3V="L" | 3.00 | 3.30 | 3.60 | V |
| Operating temperature | $T_{OP}$ | | 0 | 25 | 70 | °C |

### 3. DC characteristics

*At recommended operating conditions.

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Power consumption | $P_D$ | $V_{DD}$=5.0V, *1 | - | 150 | mW |
| | | $V_{DD}$=3.3V, *1 | - | 60 | mW |
| | | $V_{DD}$=5.0V, *2 | - | 300 | µW |
| | | $V_{DD}$=3.3V, *2 | - | 200 | µW |
| Input high level voltage (1) | $V_{IH1}$ | *3 | 2.0 | - | V |
| Input low level voltage (1) | $V_{IL1}$ | *3 | - | 0.8 | V |
| Input high level voltage (2) | $V_{IH2}$ | *4 | 0.7$V_{DD}$ | - | V |
| Input low level voltage (2) | $V_{IL2}$ | *4 | - | 0.2$V_{DD}$ | V |
| Input leakage current | $I_{LI}$ | *5 | –10 | 10 | µA |
| Input capacitance | $C_I$ | | - | 10 | pF |
| Output high level voltage (1) | $V_{OH1}$ | $I_{OH}$=–80 [µA], *6 | $V_{DD}$–1.0 | - | V |
| Output low level voltage (1) | $V_{OL1}$ | $I_{OL}$=2 [mA], *6 | - | $V_{SS}$+0.4 | V |
| Output high level voltage (2) | $V_{OH2}$ | $I_{OH}$=–80 [µA], *7 | 2.4 | - | V |
| Output low level voltage (2) | $V_{OL2}$ | $I_{OL}$=2 [mA], *7 | - | 0.4 | V |
| Output low level voltage (3) | $V_{OL3}$ | $I_{OL}$=2 [mA], *8 | - | 0.4 | V |
| Output capacitance | $C_O$ | | - | 10 | pF |
| Pull-up resistance | $R_U$ | *9 | 50 | 400 | kΩ |

Notes) *1: $f_{M1}$=33.8688MHz, normal operation

*2: Power down mode

*3: Applies to /TEST1 to TEST3, /IC, /WR/, /RD, /CS, A0 to A1, and D0 to D7.

*4: Applies to XI and 5V/3V.

*5: $V_{IN}$=0-5V. Applies to /WR, /RD, /CS, A0 to A1, D0 to D7, XI, and 5V/3V.

*6: 5V/3V="H". Applies to D0 to D7 (at output), /PDO, CLKO, BCO, LRO, WCO, and DO.

*7: 5V/3V="L". Applies to D0 to D7 (at output), /PDO, CLKO, BCO, LRO, WCO, and DO.

*8: Applies to /IRQ pin.

*9: Applies to /IC, and /TEST1 to /TEST3.

找芯片 维库一下 www.dzsc.com

## 4. AC characteristics

*At recommended operating conditions.

| Item | Symbol | Fig. | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Master clock frequency | $f_{MI}$ | Fig. 1 | - | 33.8688 | - | MHz |
| Duty 1 | D1 | | 40 | 50 | 60 | % |
| Output master clock frequency | $f_{M2}$ | Fig. 2 | - | 16.9344 | - | MHz |
| Duty 2 | D2 | | - | 50 | - | % |
| Reset pulse width | $t_{ICW}$ | Fig. 3 | $3000/f_{M1}$ | - | - | s |
| Address setup time | $t_{AS}$ | Figs. 4, 5 | 30 | - | - | ns |
| Address hold time | $t_{AH}$ | Figs. 4, 5 | 10 | - | - | ns |
| Chip select setup time | $t_{CSS}$ | Figs. 4, 5 | 5 | - | - | ns |
| Chip select hold time | $t_{CSH}$ | Figs. 4, 5 | 10 | - | - | ns |
| Write pulse width | $t_{WW}$ | Fig. 4 | 50 | - | - | ns |
| Write data setup time | $t_{WDS}$ | Fig. 4 | 10 | - | - | ns |
| Write data hold time | $t_{WDH}$ | Fig. 4 | 10 | - | - | ns |
| Read pulse width | $t_{RW}$ | Fig. 5 | 80 | - | - | ns |
| Read data access time | $t_{ACC}$ | Fig. 5 | - | - | 60 | ns |
| Read data hold time | $t_{RDH}$ | Fig. 5 | 10 | - | - | ns |
| Bit clock frequency | $f_{BC}$ | Fig. 6 | - | 48fs | - | MHz |
| Bit clock high level time | $t_{CH}$ | Fig. 6 | 110 | - | - | ns |
| Data out setup time | $t_{DOS}$ | Fig. 6 | 100 | - | - | ns |
| Data out hold time | $t_{DOH}$ | Fig. 6 | 280 | - | - | ns |
| LR clock setup time | $t_{LRS}$ | Fig. 6 | 100 | - | - | ns |
| LR clock hold time | $t_{LRH}$ | Fig. 6 | 280 | - | - | ns |
| Word clock hold time | $t_{WCH}$ | Fig. 6 | 280 | - | - | ns |

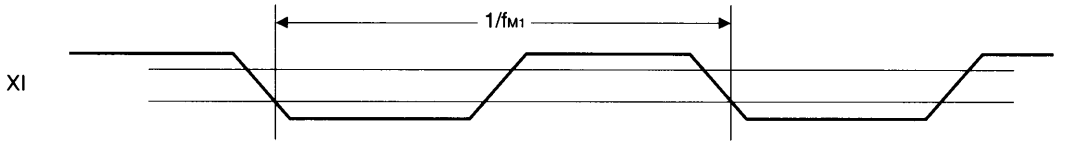



Fig. 1 Input Clock timing

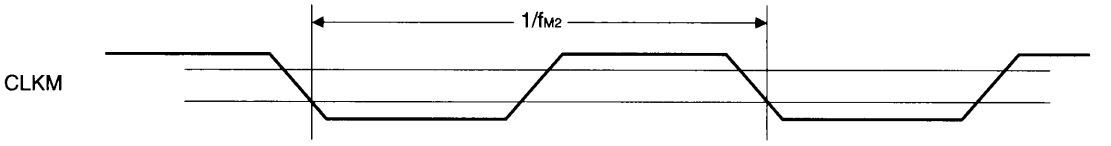



Fig. 2 Output Clock Timing

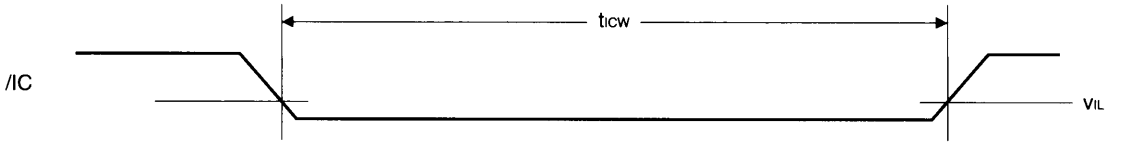



Fig. 3 Setup Pulse Width



找芯片 维库一下 www.dzsc.com

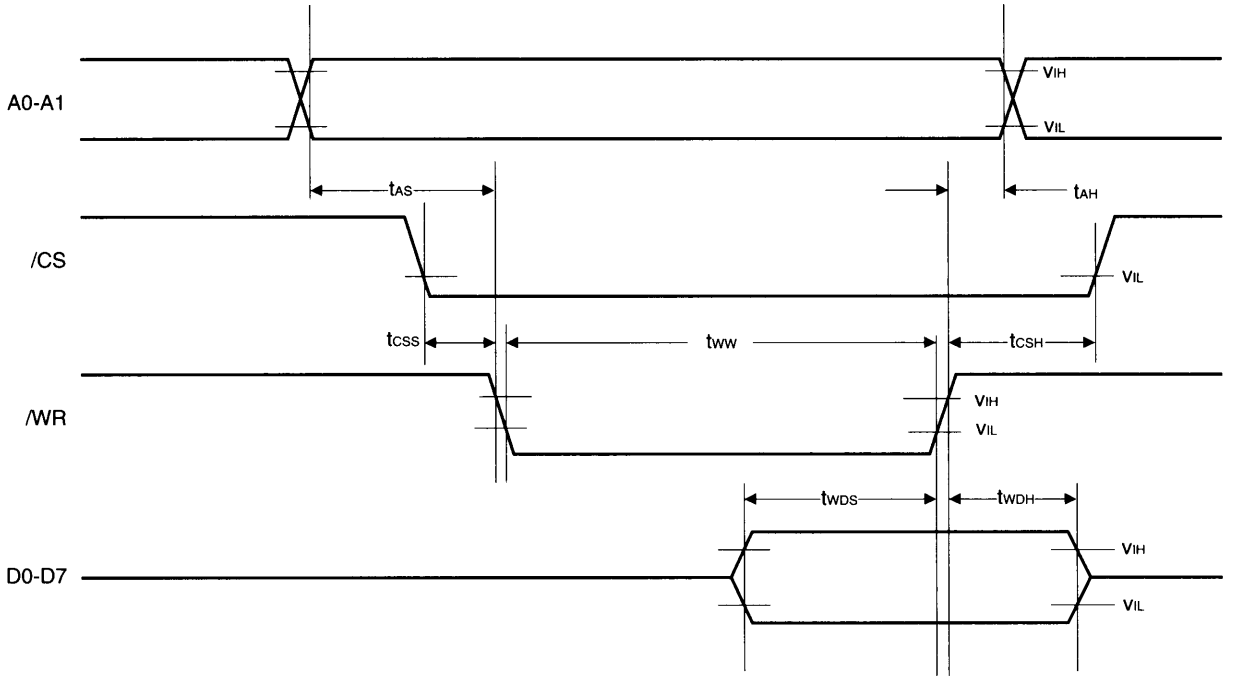



Fig. 4 CPU Write Timing

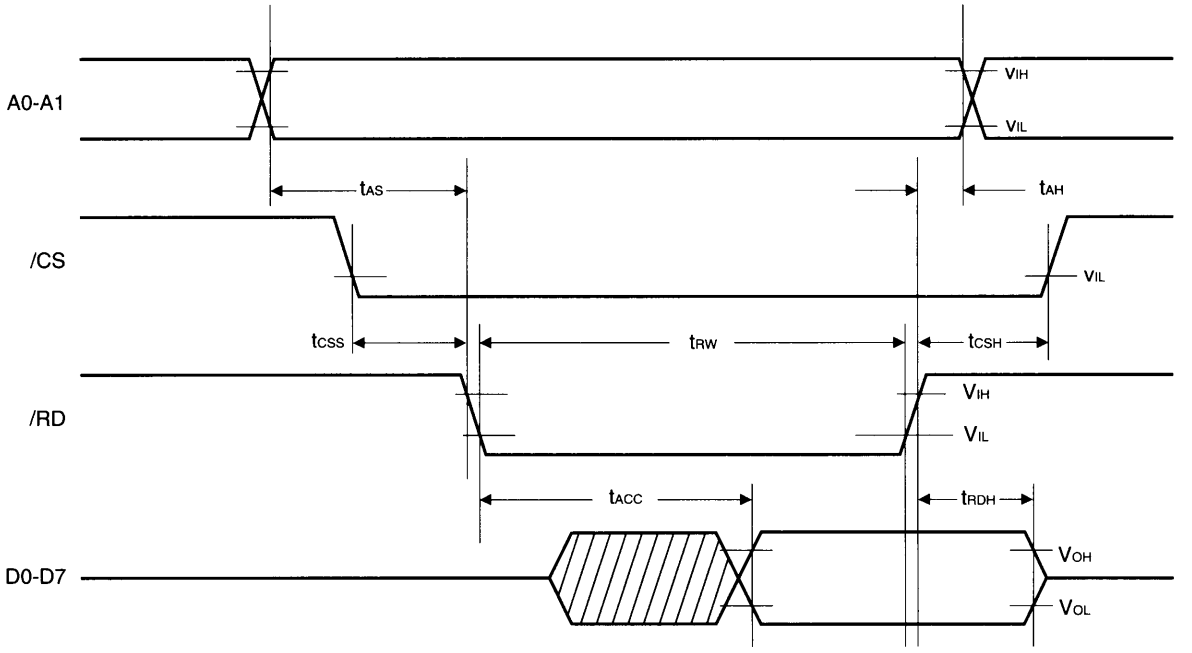



Fig. 5 CPU Read Timing

维库一下 www.dzsc.com

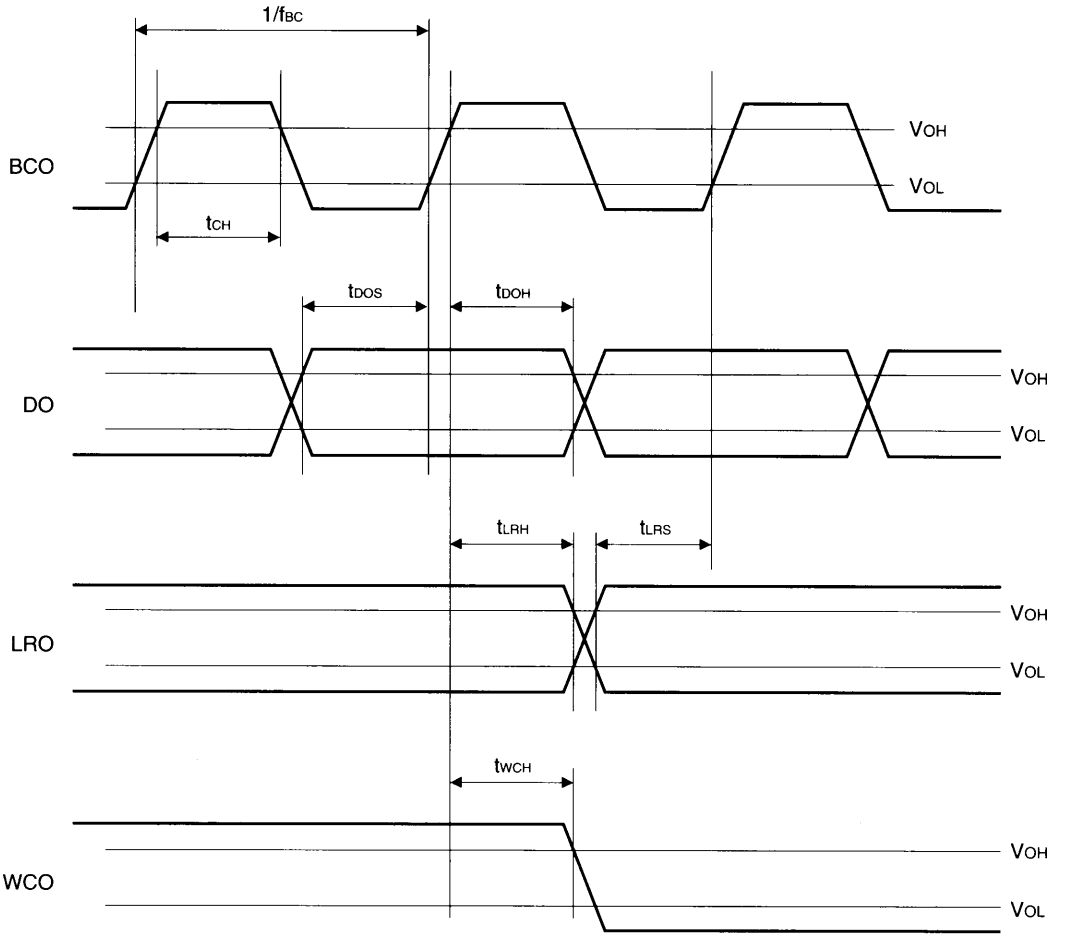



Fig. 6 DAC Interface Timing

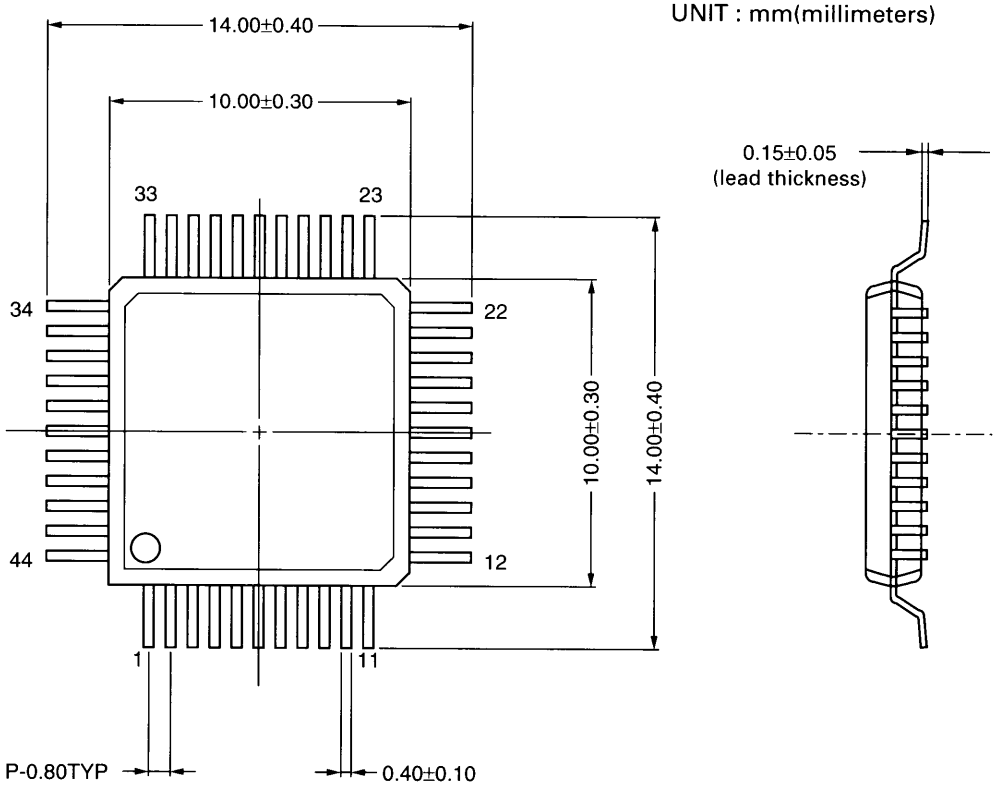


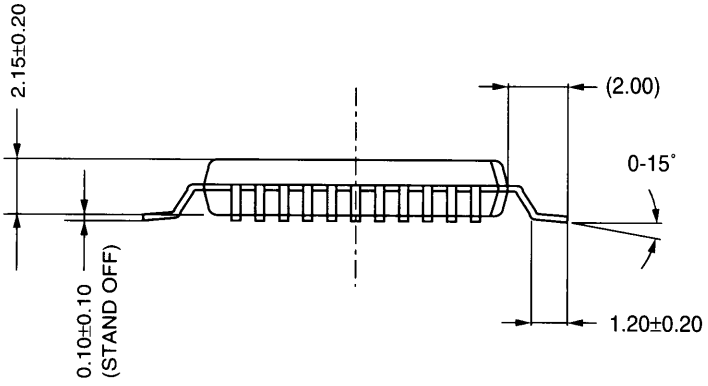
找芯片 维库一下 www.dzsc.com

## ■ EXTERNAL DIMENSIONS

### • YMF289B-F (44QFP)

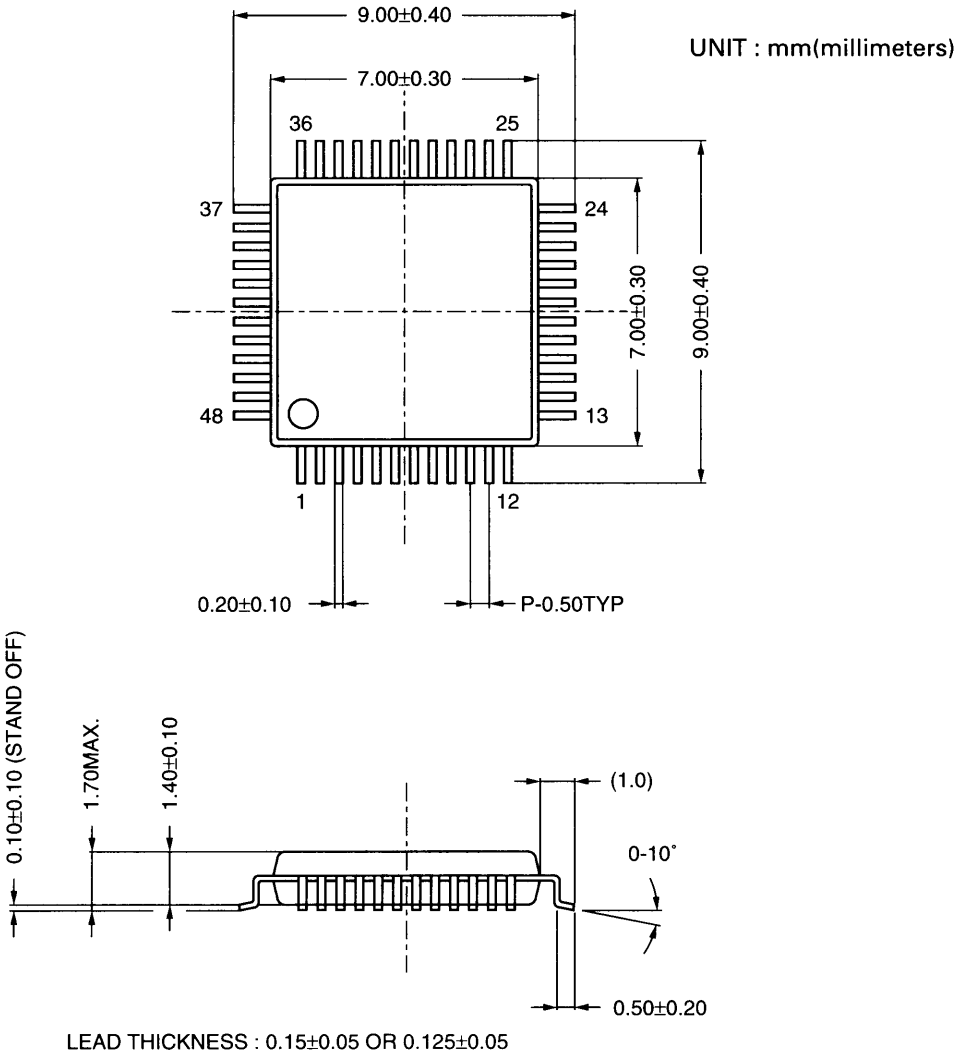
UNIT : mm(millimeters)




找芯片 维库一下 www.dzsc.com

- **YMF289B-S (48SQFP)**






找芯片 维库一下 www.dzsc.com

找芯片 维库一下 www.dzsc.com

## IMPORTANT NOTICE

1. Yamaha reserves the right to make changes to its Products and to this document without notice. The information contained in this document has been carefully checked and is believed to be reliable. However, Yamaha assumes no responsibilities for inaccuracies and makes no commitment to update or to keep current the information contained in this document.

2. These Yamaha Products are designed only for commercial and normal industrial applications, and are not suitable for other uses, such as medical life support equipment, nuclear facilities, critical care equipment or any other application the failure of which could lead to death, personal injury or environmental or property damage. Use of the Products in any such application is at the customer's sole risk and expense.

3. YAMAHA ASSUMES NO LIABILITY FOR INCIDENTAL, CONSEQUENTIAL OR SPECIAL DAMAGES OR INJURY THAT MAY RESULT FROM MISAPPLICATION OR IMPROPER USE OR OPERATION OF THE PRODUCTS.

4. YAMAHA MAKES NO WARRANTY OR REPRESENTATION THAT THE PRODUCTS ARE SUBJECT TO INTELLECTUAL PROPERTY LICENSE FROM YAMAHA OR ANYTHIRD PARTY, AND YAMAHA MAKES NO WARRANTY OR REPRESENTATION OF NON-INFRINGEMENT WITH RESPECT TO THE PRODUCTS. YAMAHA SPECIFICALLY EXCLUDES ANY LIABILITY TO THE CUSTOMER OR ANY THIRD PARTY ARISING FROM OR RELATED TO THE PRODUCTS' INFRINGEMENT OF ANY THIRD PARTY'S INTELLECTUAL PROPERTY RIGHTS, INCLUDING THE PATENT, COPYRIGHT, TRADEMARK OR TRADE SECRET RIGHTS OF ANY THIRD PARTY.

5. EXAMPLES OF USE DESCRIBED HEREIN ARE MERELY TO INDICATE THE CHARACTERISTICS AND PERFORMANCE OF YAMAHA PRODUCTS. YAMAHA ASSUMES NO RESPONSIBILITY FOR ANY INTELLECTUAL PROPERTY CLAIMS OR OTHER PROBLEMS THAT MAY RESULT FROM APPLICATIONS BASED ON THE EXAMPLES DESCRIBED HEREIN. YAMAHA MAKES NO WARRANTY WITH RESPECT TO THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR USE AND TITLE.

AGENCY

YAMAHA CORPORATION

Address inquiries to :
Semiconductor Sales & Marketing Department

■Head Office 203, Matsunokijima, Toyooka-mura,
Iwata-gun, Shizuoka-ken, 438-0192
Tel. +81-539-62-4918 Fax. +81-539-62-5054

■Tokyo Office 2-17-11, Takanawa, Minato-ku,
Tokyo, 108-8568
Tel. +81-3-5488-5431 Fax. +81-3-5488-5088

■Osaka Office Namba Tsujimoto Nissei Bldg, 4F
1-13-17, Namba Naka, Naniwa-ku,
Osaka City, Osaka, 556-0011
Tel. +81-6-6633-3690 Fax. +81-6-6633-3691

■U.S.A Office YAMAHA Systems Technology.
100 Century Center Court, San Jose, CA 95112
Tel. +1-408-467-2300 Fax. +1-408-437-8791

prohibited © 1987 YAMAHA CORPORATION

0.3K-0324 Printed in Japan 94.12

找芯片 维库一下 www.dzsc.com